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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,331	09/08/2003	William C. Moyer	SC13074TH	1204

23125 7590 02/16/2006

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,331	MOYER, WILLIAM C.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see continue page*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

06/14/05, 03/21/05, 09/08/03

1. Claims 1-22 are presented for examination. Applicant is reminded that the last page of 1449 sent by fax on 03/21/05 at 10:18 has been missing. However, there is another IDS sent by fax on 03/21/05 at 12:40. Applicant is suggested to confirm that whether these two copies should be the same in the next response.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/657,797. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the copending claim 1 does not recite the the transfer between the memory and at least two registers as claimed, it would have

been obvious to one of ordinary skill in the art to transfer betrween the memory and two registers as claimed because the copending claim 1 also taught a trtansfer between the memory and at least one register (see copending claim1), which would have been recognizable by one of skill in the art that more number of registers was also applicable in the copending case for transfer purpose , and the at least one register should not be confined to be used for just one register, rather more registers should be applied.

3. Claim 1 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/657,510 Although the conflicting claims are not identical, they are not patentably distinct from each other because although the copending claim 1 did not recite the number of data elements to be transferred as claimed, it would have been obvious to one of ordinary skill in the art to include the number of data elements to be transferred because the copending claim 1 also taught the determination of the data element size in a register (see copending claim1), which would have been recognizable by one of ordinary in the art that konwing the length of the register , data number could be determined from the data size, for example, DN = DS/ length register, therefore the data number could have been have determined using the starting location value of the register of a given data element size.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida (5,870,596).

5. As to claim 1,5,8,13, 10,15, Yoshida disclosed

a) a memory for storing operands (see how the load and store transfer operand data to/from the memory stack in col.9, lines 65-67, col.10, lines 1-11);

b) a plurality of general purpose registers wherein each general purpose register holds multiple data elements (see the plurality of registers in col.9, lines 65-67, col.10, lines 1-11, see the bytes in each registers); and

c) processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers (see any two of the registers R1,R4,R5,R6,R7,R8 in fig.33) wherein the at least one or more instructions specifies a number of register elements (see the loading of 4 bytes

according to the internal code LDM1 to R1 in col.24, lines 14 –21, as to which element ,see the lower byte) to be transferred between each of the at least two of the plurality of general purpose registers and the memory (see also the 4 byte loaded into register R4 in col.24, lines 45-50).

6. As to claims 2,6, Yoshida also specified which of the register elements to load or store (see the load and store instructions LDM and STM to pop or push data bytes in col.23, lines 15-23).

7. As to claims 3, 7,9, 14, Yoshida did not explicitly show to fill the unspecified data element with a predetermined value as claimed. However, the examiner holds that filling any register including specified and unspecified data elements with a predetermined value is inherent feature of every system. For example, a bit (either specified or unspecified) in a register should be filled with either "0" or "1". The "0" and "1" is a predetermined value.

8. As to claims 4, 10, The examiner also holds that if all bits are zero the value has to be zero.

9. As to claims 11, 12, Yoshida was applicable to both contiguous and discontinuous (see the fetch data address incremented by 4 in col.24, lines 8-29).

10. As to claim 16, Yoshida also included total byte greater than the data elements to be transfer to each of the registers (se the six bytes from the memory area onto six registers in col.22, lines 64-67, col.23, lines 1-14).

11. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hinds et al. (6,170,001).

12. As to claims 1, 5,8, 10,13,15, Hinds taught at lest :

a) a memory for storing operands (see transfer between register bank and memory in col.2, lines 29-30);

b) a plurality of general purpose registers wherein each general purpose register holds multiple data elements (single precision and double precision) ; and processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers (see either the RS or RD operands) wherein the at least one or more instructions specifies a number of register elements (see the number of odd number data words in col.2, ,lines 60-67, see also the data type bit used as specifying the single or double data size in col.10, lines 54-64) to be transferred between each of the at least two of the plurality of general purpose registers and the memory (see col.20, lines 11-48 for the detail of operand data elements in a bank of registers).

13. As to claims 2,6, Hinds also specified which of the register elements to load or store (see the load and store instructions with specified register in col.7, lines 16-26).

14. As to claims 3,4 7,9, 10, 14, Hinds also filled the unspecified data element with a predetermined value (see the logic 0 stored into one of the uninitiolized data slots in col.12, lines 53-67).

15. As to claims 11, 12, Hinds was applicable to both contiguous and discontinuous (see the single and pair of data slots in col.12, lines 55-67).

16. As to claim 16, Hinds also included total number (see the DH and DL) to be transferred greater than the number of data elements (see each of the DH and DL) to be transfer to each of the registers (see each entry in register 200 in fig.15).

17. As to clams 17,18, Hinds also included total number of data element (see single S) less than each of the registers (see the double s in a single register in fig.15) , any remaining data element was filed with a predetermined value (see the logic 0 stored in register 200 in col.12, lines 55-67) .

18. Claims 1,5,8, 10,15, are rejected under 35 U.S.C. 102(b) as being anticipated by Inagami et al. (4,760,545).

19. As to claim 1,5,8,10,13, 15, Inagami disclosed :

a) a memory for storing operands (see the main memory in figs.1 and 2, col.1, lines 59-68);

b) a plurality of general purpose registers wherein each general

purpose register holds multiple data elements (see the plurality of registers vector registers); and

c) processor circuitry for executing one or more instructions, at least

one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers (see transfer of vector data elements in col.1, lines 59-68, see also the loading of data elements in col.2, lines 22-56, col.4, lines 11-68, see the operands in col.5, lines 1-4) wherein the at least one or more instructions specifies a number of register elements (see fig.4b , L being the number of vector elements to be transferred, see also the number specified by instruction in col.6, lines 52-68) to be transferred between each of the at least two of the plurality of general purpose registers and memory.

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Honma (4,903,195) is cited for the teaching of the specifying total number of data elements to be transferred see col.2, lines 63-68, col.3, lines 1-8);

b) Apperley is cited for the teaching of specifying number of data elements to be transferred (see col.14, lines 40-53).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162.

The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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